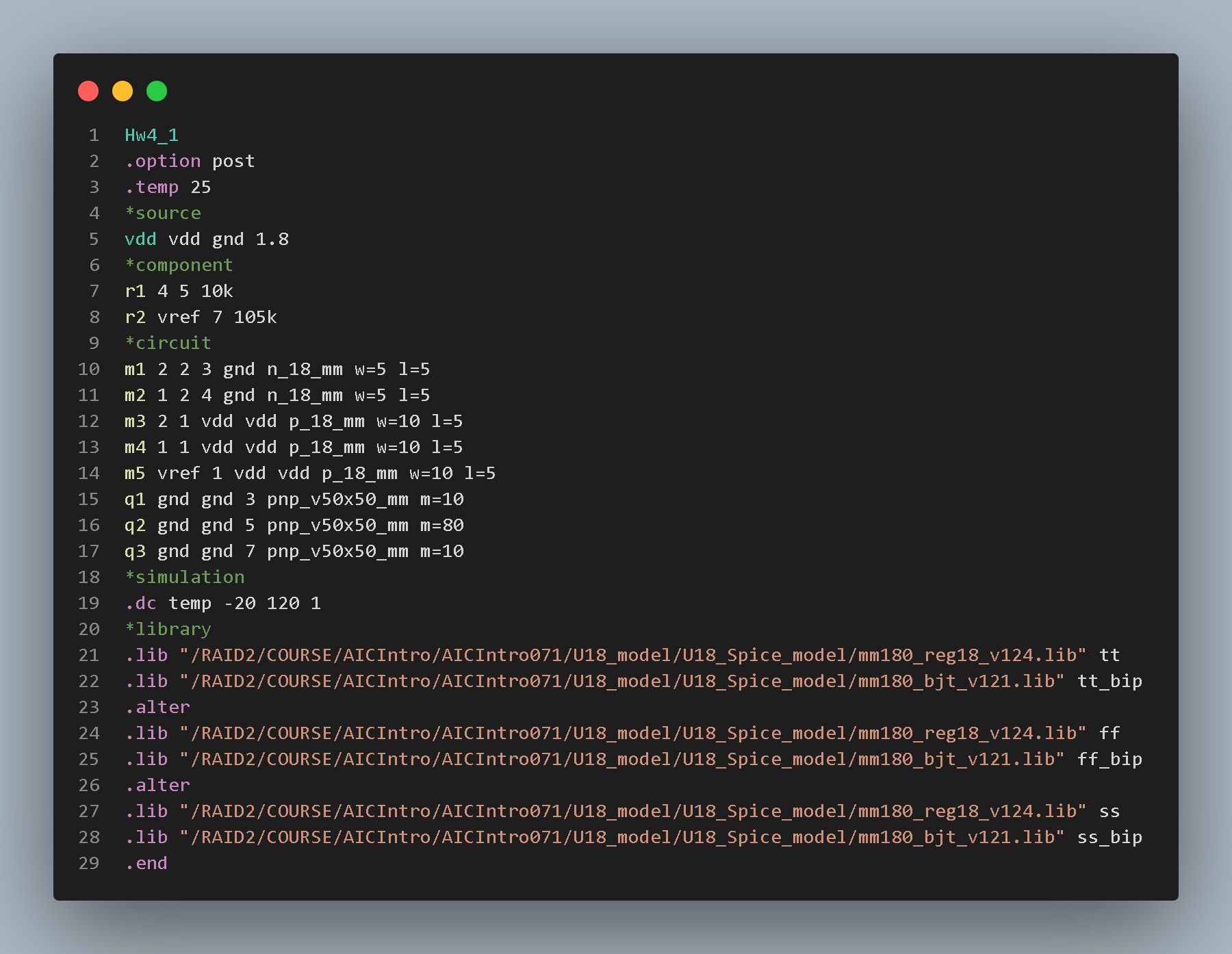
HSPICE Homework #4 of「類比積體電路導論」

As the Transistor level implementation of a bandgap reference shown below, please perform HSPICE simulations with the device parameters of U18 0.18µm CMOS technology.

From your simulation results,

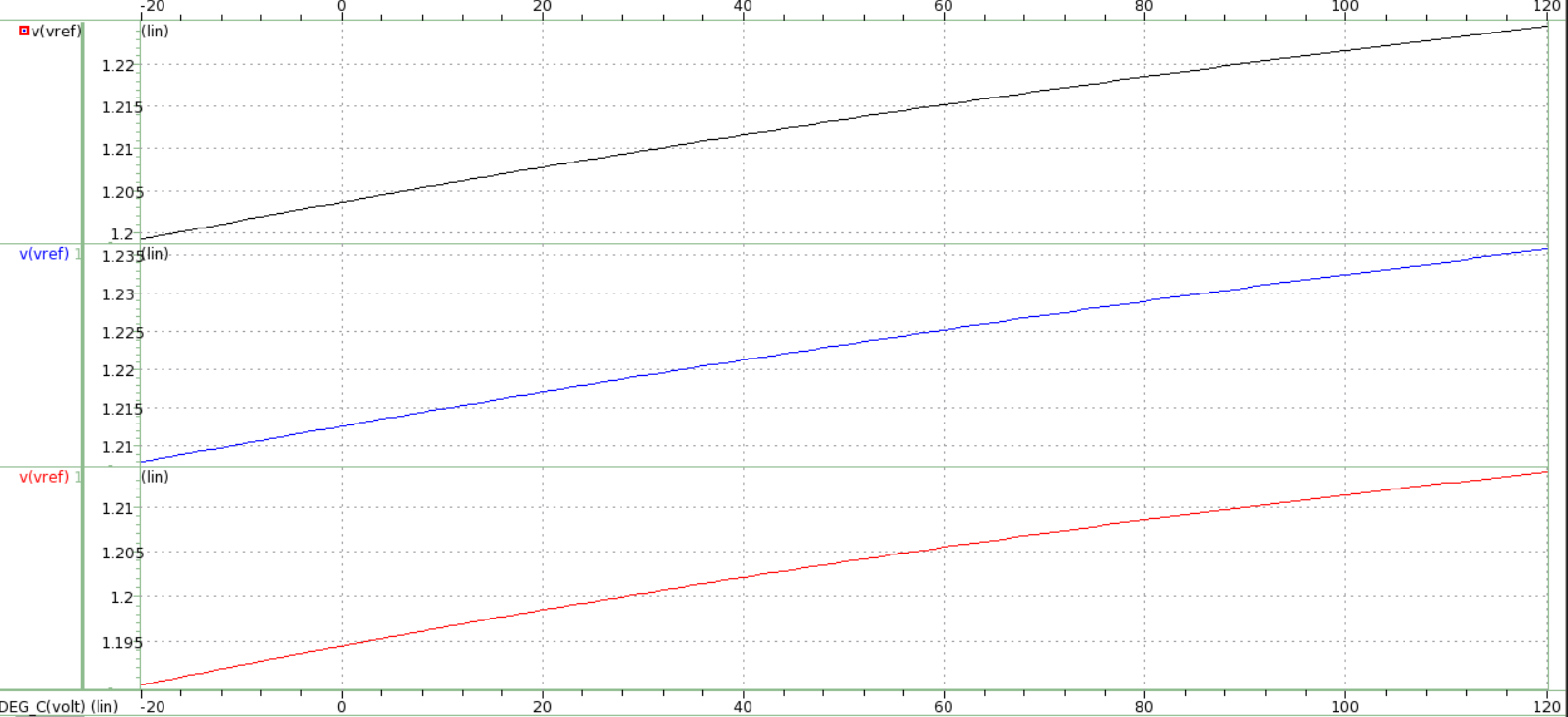
1. Plot(x,y)=(Temperature-20°C~120°C, 𝑉𝑅𝐸𝐹) at TT, FF and SS corners when VDD=1.8 V. Please explain the reasons which cause such differences.

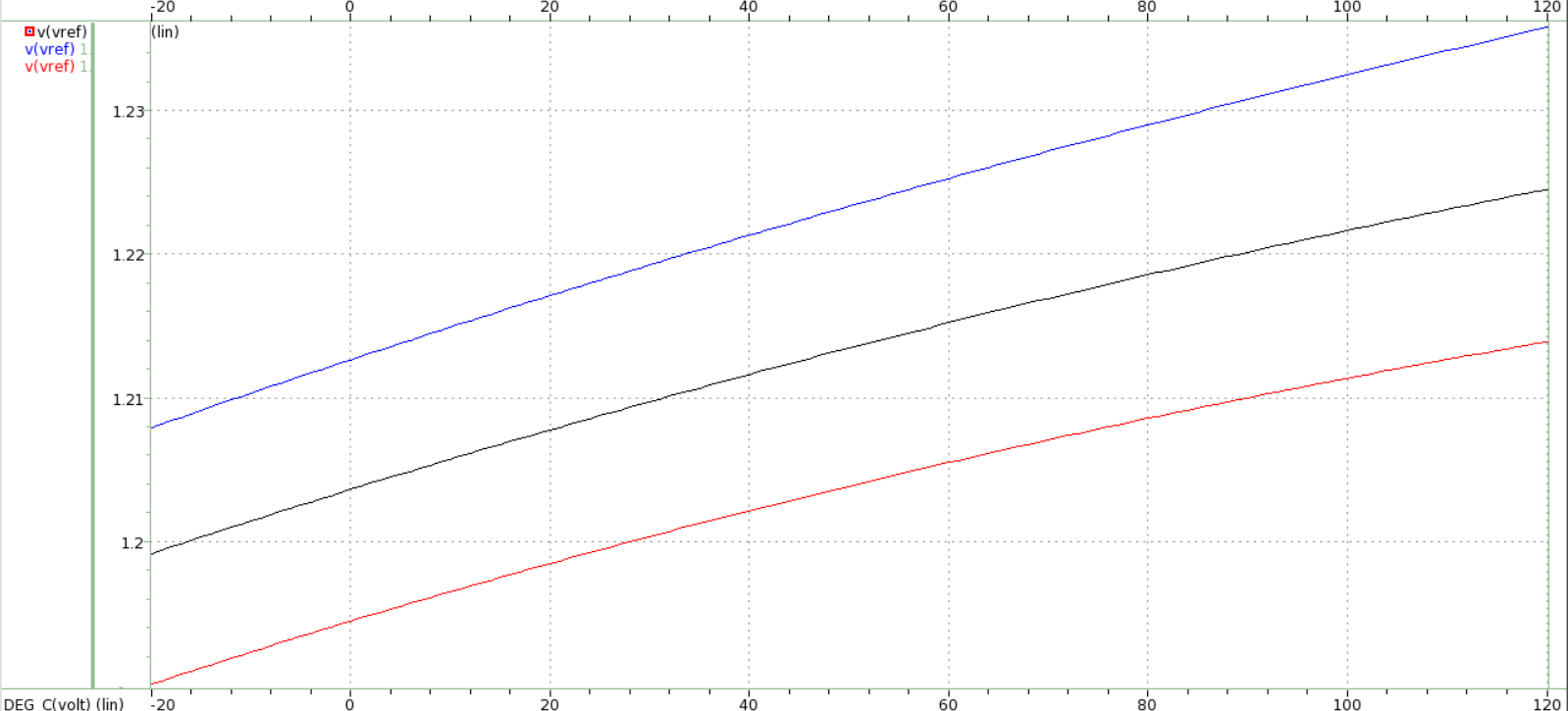


Black line: tt corner

Blue line: ff corner

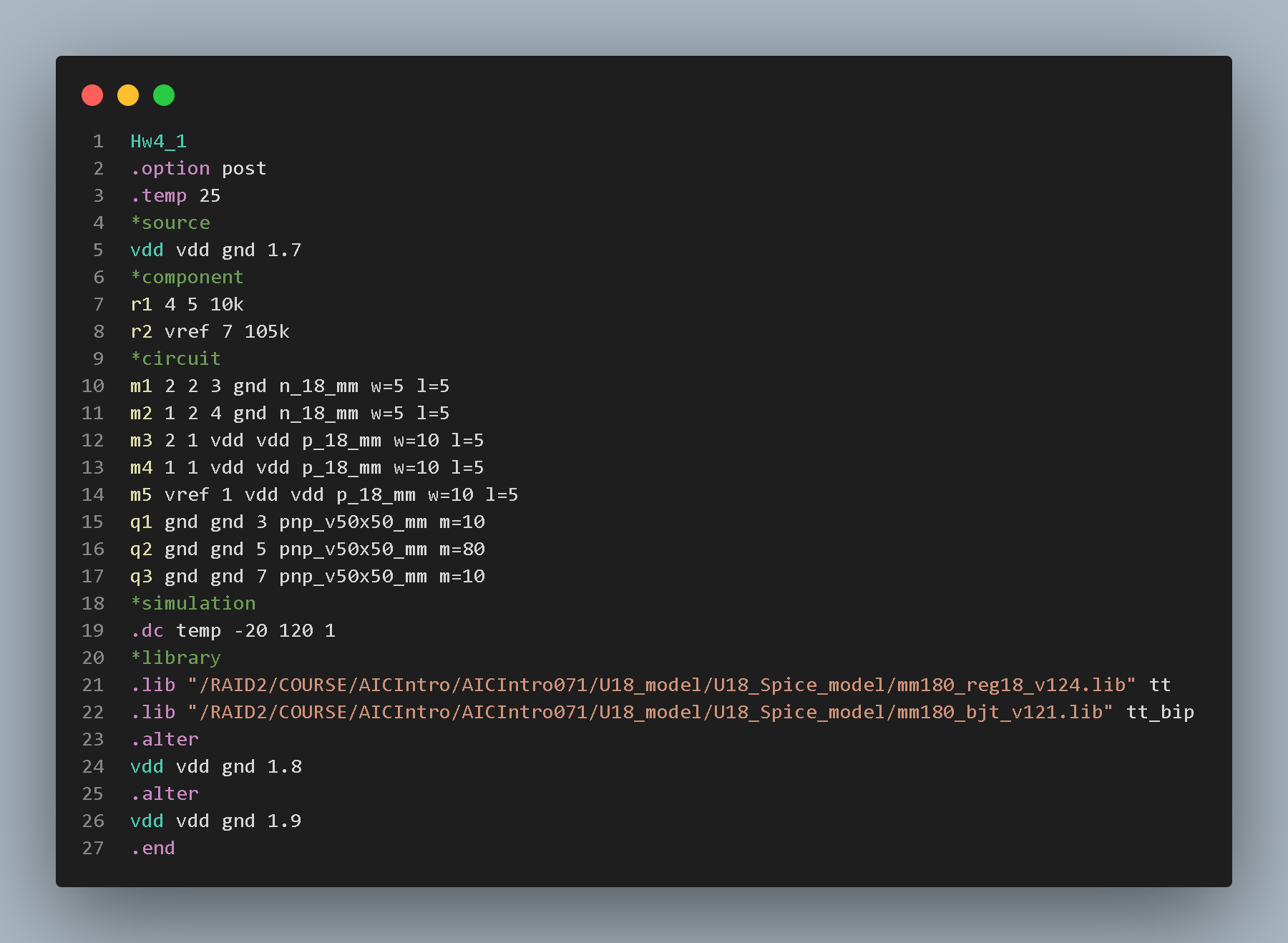
Red line: ss corner





By observing the result above, it is found that the slopes of the three corners (V/℃) are approximately the same, the differences between them are the DC bias. As FF corner flows through a bigger current and SS corner flows through a smaller corner, the Vref of FF corner is larger than that of TT corner, and the vref of TT corner is larger than that of the SS corner. However, there’re just a little gap between three.

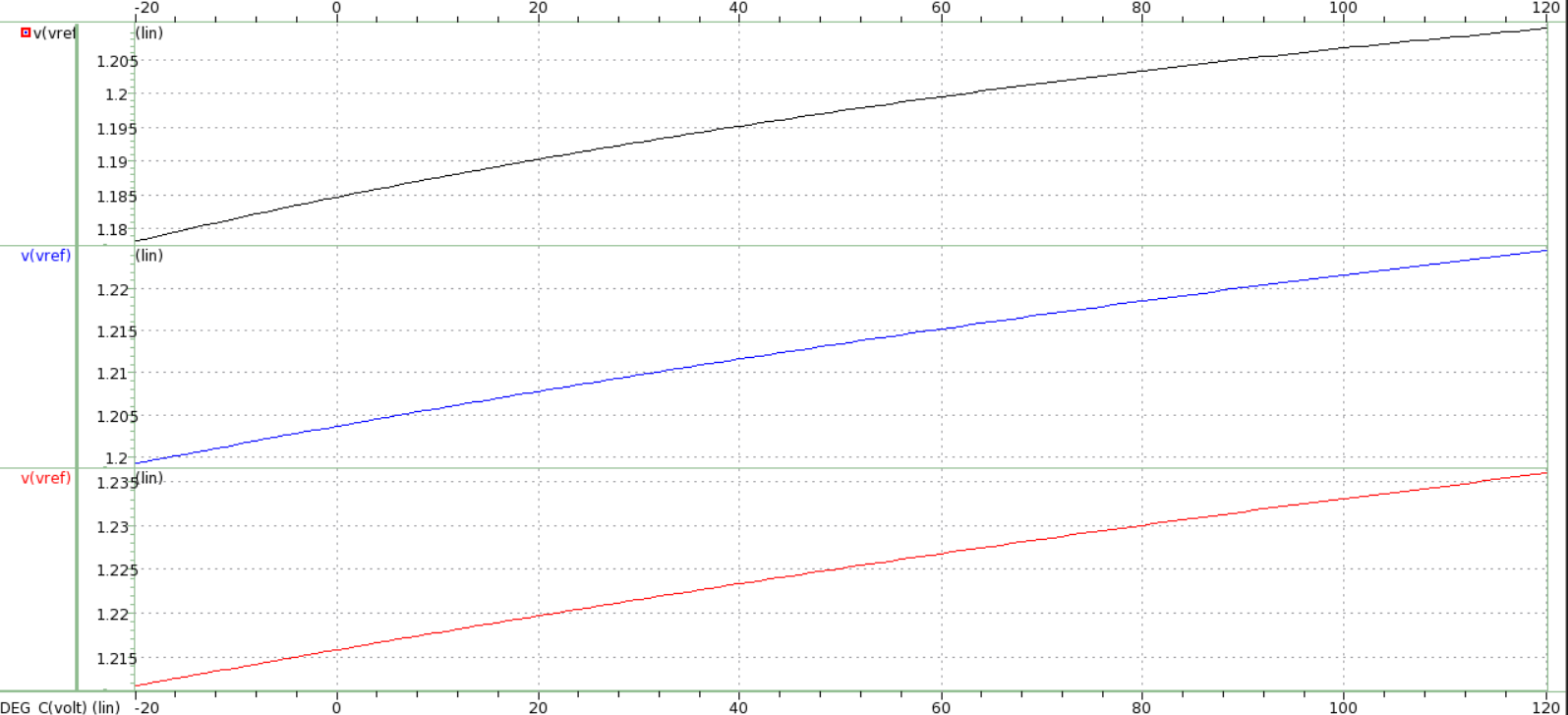
1. Plot(x,y)=(Temperature-20°C~120°C, 𝑉𝑅𝐸𝐹) at TT corner when VDD=1.7/1.8/1.9 V. Please explain the reasons why VDD makes an impact on 𝑉𝑅𝐸𝐹.

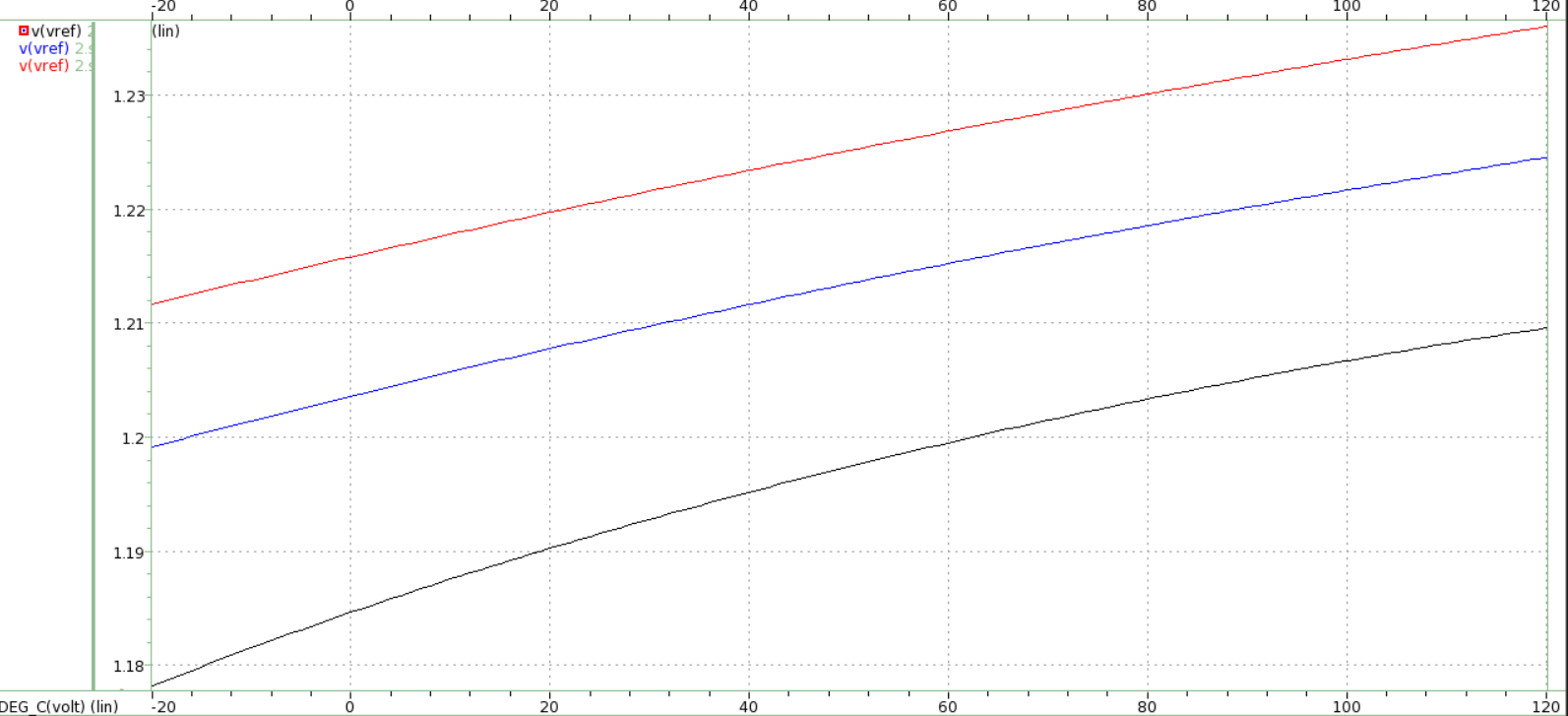


Black line: 1.7V

Blue line: 1.8V

Red line: 1.9V

****

****

It is found that the vref When VDD=1.8V and VDD=1.9V have approximately the same slope(V/℃). However, the vref when VDD=1.7V have a larger slope. The reason is that the formula Vptat=R2/R1\*Vt\*ln(n). The term Vt is proportional to the VDD. That is, the larger VDD is, the larger Vt increase. And the larger Vptat is, the larger Vref is. And in the ideal situation when Ro is infinite, the change of VDD will cause a change in Iout. However, the RO in the 18\_mm.lib is not infinite. Therefor, VDD will slightly influence Iout.